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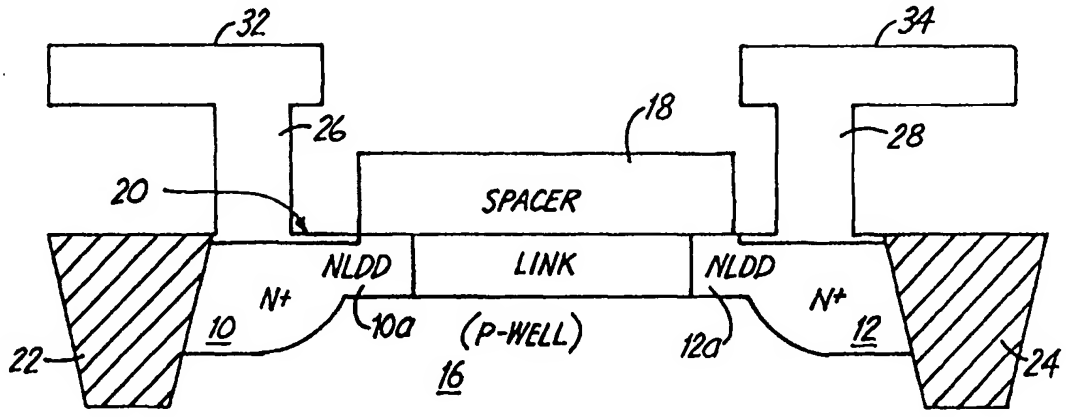
(54) Title: SEMICONDUCTOR DEVICE WITH TRANSPARENT LINK AREA FOR SILICIDE APPLICATIONS AND FABRICATION THEREOF



(57) Abstract

Useful to inhibit reverse engineering, semiconductor devices and methods therefor include formation of two active regions over a substrate region in the semiconductor device. According to an example embodiment, a dopable link, or region, between two heavily doped regions can be doped to achieve a first polarity type, with the two heavily doped regions of the opposite polarity. If dictated by design requirements, the dopable region is adapted to conductively link the two heavily doped regions. A dielectric is formed over the dopable region and extends over a portion of each of the two heavily doped regions to inhibit silicide formation over edges of the dopable region. In connection with a salicide process, a silicide is then formed adjacent the dielectric and formed over another portion of the two heavily doped regions.

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SEMICONDUCTOR DEVICE WITH TRANSPARENT LINK AREA FOR SILICIDE APPLICATIONS AND FABRICATION THEREOF

Field of the Invention

The present invention relates generally to semiconductor devices and semiconductor manufacturing and, more particularly, to semiconductor devices using silicide processes generally and in connection with efforts to inhibit reverse engineering.

Background of the Invention

The electronics industry continues to rely upon advances in semiconductor technology to realize higher-functioning devices in more compact areas. For many applications, realizing higher-functioning devices requires integrating a large number of electronic devices into a single silicon wafer. As the number of electronic devices per given area of the silicon wafer increases, the manufacturing process becomes more difficult.

A large variety of semiconductor devices have been manufactured having various applications in numerous disciplines. Such silicon-based semiconductor devices often include metal-oxide-semiconductor (MOS) transistors, such as p-channel MOS (PMOS), n-channel MOS (NMOS) and complementary MOS (CMOS) transistors, bipolar transistors, BiCMOS transistors, etc.

Each of these semiconductor devices generally includes a semiconductor substrate on which a number of active devices are formed. The particular structure of a given active device can vary between device types. While the particular structure of a given active device can vary between device types, a MOS-type transistor generally includes heavily doped diffusion regions, referred to as source and drain regions, and a gate electrode that modulates current flowing in a channel between the source and drain regions.

One important step in the manufacture of such devices is the formation of isolation areas to electrically separate electrical devices or portions thereof that are closely integrated in the silicon wafer. Typically, current does not flow between active regions of adjacent MOS-type transistors. However, in certain circuit designs it is desirable to electrically link source/drain diffusions of adjacent MOS-type

transistors. Such linking is useful in various circuit design applications including, for example, adjacent transistor circuits requiring resistive transistor intercoupling.

In circuit applications involving two diffusion regions of the same polarity type, such as two P+ doped adjacent regions in an N-well substrate area, the portion of the substrate area between the two adjacent regions can be used as an electrical insulator. More specifically, each heavily doped diffusion region and a portion of adjacent substrate act as a reverse-biased diode blocking the flow of electrons between the two diffusions. Conversely, the portion of the substrate area between the two adjacent regions can also be implemented to act as an electrical conductor. One way to implement such conduction is to effect the same polarity in the portion of the substrate area between the two adjacent regions as the polarity of the two adjacent regions. Accordingly, each adjacent heavily doped region can be doped simultaneously with the portion of the substrate area between the two adjacent regions to overcome the reverse-biased diode effect.

For many designers, linking two active regions of the same polarity type in this manner is desirable for preventing reverse engineering by competitors. Reverse engineering involves the use of analytical techniques, such as scanning-electron microscopy, to determine the design of an integrated circuit including identification of electrical connections between active regions. For many analytical techniques, including scanning-electron microscopy, linking and blocking connectivity between two active regions of the same polarity type, in the manner described above, appears identical and thereby undermines the typical reverse-engineering effort.

This approach is not readily achievable for all circuit architectures, particularly those involving salicide processes. Salicide processing refers to self-aligned silicide processing; in which metal is heat-reacted with silicon to form "silicide" over an active region to form contact regions over the silicide with minimal masking steps. In a salicide process, siliciding two heavily doped regions of the same polarity normally results in silicide forming over the portion of the substrate area between the two adjacent regions which, in turn, results in shorting the two heavily doped regions. Because the two adjacent regions are linked by the detectable silicide, typical reverse-

engineering efforts can readily detect whether or not the adjacent heavily doped regions are electrically linked.

Summary of the Invention

The present invention is exemplified in a number of implementations, some of which are summarized below. According to one embodiment, a method of fabricating a semiconductor device, includes first forming a dopable region between two heavily doped regions over a substrate region in the semiconductor device, with the substrate region doped to achieve a first polarity type, and with the two heavily doped regions doped to achieve a second polarity type that is opposite the first polarity type. The dopable region is adapted to selectively link the two active regions when doped to achieve the second polarity type. Further, over the dopable region and extending over a portion of each of the two heavily doped regions, a dielectric is formed that is adapted to inhibit silicide formation over edges of the dopable region and the structure is silicided adjacent the dielectric over another portion of at least one of the two heavily doped regions.

In another embodiment of the present invention, a semiconductor device, comprises: two heavily doped regions over a substrate region in the semiconductor device; a dopable region between the two heavily doped regions, the substrate region doped to achieve a first polarity type, wherein the two active regions are doped to achieve a second polarity type that is opposite the first polarity type, and wherein the dopable region is adapted to selectively link the two heavily doped regions when doped to achieve the second polarity type; a dielectric formed over the dopable region and extending over a portion of each of the two active regions, the dielectric adapted to inhibit silicide formation over edges of the dopable region; and a silicide formation adjacent the dielectric over another portion of at least one of the two heavily doped regions.

The above summary of the present invention is not intended to describe each illustrated embodiment or every implementation of the present invention. The figures and the detailed description that follow more particularly exemplify these embodiments.

Brief Description of the Drawings

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 illustrates a cross-sectional view of semiconductor structure including two adjacent heavily doped regions of the same polarity type, according to an example embodiment of the present invention;

FIGs. 2 through 6 are cross-sectional views illustrating process steps useful in forming the semiconductor structure of FIG. 1, in accordance with the present invention; and

FIG. 7 is a top-down view showing the architecture of the semiconductor structure of FIG. 1, in accordance with another example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description of the Various Embodiments

The present invention has been found to be particularly advantageous in applications where it is desirable inhibit or prevent reverse-engineering efforts. While the present invention is not necessarily limited to this environment, an appreciation of various aspects of the invention is best gained through a discussion of example of such applications.

One particular example implementation of the present invention is directed to a semiconductor device and its fabrication. The semiconductor device is manufactured to include a diffusion region separating two active regions over a substrate region in the semiconductor device. The substrate region is of one polarity type, N or P, and each of the two heavily doped regions is the same opposite polarity

type, P+ or N+, respectively, with a portion of the heavily doped region extending into the substrate. Over the diffusion region and a portion of each of the two active regions, a dielectric (such as a spacer oxide or other insulative material) is formed to inhibit silicide formation over edges of the dopable region. Metal is applied and a silicide is formed adjacent the dielectric over another portion of one or both two active regions.

Depending on the design requirements, the active regions can relate to one another electrically as: inter-linked, for example, by doping the diffusion region to achieve the same polarity type as the active regions; isolated from one another by blocking this diffusion region, for example, by appropriately masking to block the doping/implanting step; or resistively-linked, for example, by doping the diffusion area selectively (*e.g.*, lightly relative to the doping concentration of the respective active areas on either side of the diffusion area). In each instance, the structure will appear identical under a microscope.

Turning now to the drawings, FIG. 1 depicts a cross-sectional view of another example embodiment of a semiconductor structure, also according to the present invention. The semiconductor structure of FIG. 1 includes two adjacent active regions 10 and 12 doped N+, with a diffusion area 14 therebetween, a P+ well 16 underneath, and an oxide spacer 18 atop. Field oxide regions 22 and 24 are depicted on either side of the active regions 10 and 12 in this example structure.

Nearest the diffusion area 14, portions of each of two adjacent active regions 10 and 12 include lightly doped (e.g., NLDD) areas 10a and 12a, respectively. The NLDD areas 10a and 12a extend beneath the oxide spacer 18 to prevent shorting of the adjacent N+ region 10 or 12 to the P well 16, and with sufficient overlap between the oxide spacer 18 and the NLDD areas 10a and 12a to allow for mask alignment tolerances and loss of spacer during subsequent processing. According to one application/circuit-design, the diffusion area 14 acts as an insulator in a manner similar to two reverse-biased diodes. Alternatively, a link is formed between the two NLDD areas 10a and 12a by implanting NLDD under the entire spacer. As a further alternative, a resistive link between the two NLDD areas 10a and 12a can be achieved by implanting NLDD in a selective manner to define the desired resistive

characteristics in the link area. For example, the implant can be implemented selectively to achieve a complete link by evenly doping under the entire spacer, or selectively to achieve a resistive link by doping with selective concentrations and/or areas under the spacer. With the dopant concentration, or lack thereof, undetectable by microscopy, the structure serves to frustrate conventional reverse-engineering efforts.

Metal is applied and a silicide 20 is formed adjacent the oxide spacer 18 over both active regions 10 and 12. Contacts 26 and 28 are then formed after formation of the silicide, and connections 32 and 34 are then made to the contacts 26 and 28 via metal lines.

FIGs. 2 through 6 illustrate an example set of process steps useful in forming the semiconductor structure of FIG. 1, also in accordance with the present invention. In one example implementation, these process steps are used in connection with a standard 0.25 micron process flow. FIG. 2 depicts the formation of the LDD mask 50 in the form of a line of resist, in the situation where the diffusion area is not doped to link the active areas 10a and 12a of FIG. 1. The diffusion area may also be doped to link the active areas 10a and 12a, for example, by eliminating this step depicted in FIG. 2. In FIG. 3, after removing the resist, a spacer mask and an etch step are used to define an oxide region, or oxide spacer 18, with sufficient overlap to isolate the diffusion area to allow for mask alignment and spacer loss in the areas 10a and 12a (for the case of isolated nodes or active-regions). Next, an N+ implant is used to define the heavier-doped N+ regions 10 and 12 as shown in FIG. 4. As depicted in FIG. 5, a salicide processing step leaves a layer of silicide 20 on the active regions 10 and 12, with the oxide spacer 18 used to block silicide formation that would otherwise short the N+ regions together across the top of the diffusion area. As show in FIG. 6, the contacts and metal connections are formed to complete this stage of processing, and the device is connected to the appropriate nodes as defined by the circuit specifications.

FIG. 7 is a top-down view showing the architecture of the semiconductor structure of FIG. 1, in accordance with another example embodiment of the present invention. The dotted-line region, depicted as 60, shows the area where the LDD

implant was blocked, in the instance where no link was formed between the two active regions.

In one example application involving a standard 0.25 micron process flow, a minimum link size includes one square of non-silicided LDD diffusion, providing a resistance of about 1000 Ohms. Greater or lesser resistances can of course be realized, for example, by changing the width of the link.

In another example process, also consistent with the present invention, a salicide-exclusion process involves depositing a dieletric film and then etching the film immediately prior to silicide formation. In this instance, the dielectric layer is designed to overlap the heavily doped regions, thereby eliminating any need for a lightly doped implant when a link between the active regions is unnecessary.

Accordingly, the present invention has a number of advantageous aspects. For instance, the implemented function of the link area in each of the above-discussed embodiments is undetectable using conventional microscopy. Another significant advantage is that the link area can be implemented as a conductive link or resistive link without adding steps to a conventional manufacturing process. For example, the conductive/resistive link can be implemented during the implant step(s) for the active region. Implant steps for building active regions is conventional and therefore adds no further significant cost or delay.

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes may be made thereto. Another variation, for example, involves use of only one side of the spacer to block silicide-related shorting. These changes and other departures from the above discussion of example embodiments are within the spirit and scope of the present invention, as set forth in the following claims.

What is claimed is:

1. A semiconductor device, comprising:

two regions (10, 12) over a substrate region in the semiconductor device;

a dopable region between the two regions, the substrate region doped to achieve a first polarity type, wherein the two regions are doped to achieve a second polarity type that is opposite the first polarity type, and wherein the dopable region is adapted to selectively link the two regions (10, 12) when doped to achieve the second polarity type;

a dielectric (18) formed over the dopable region and extending over a portion of each of the two regions, the dielectric adapted to inhibit silicide formation over edges of the dopable region; and

a silicide formation (20) adjacent the dielectric over another portion of at least one of the two regions.

2. A semiconductor device, according to claim 10, further including the dopable region being doped to conductively link the two regions.

3. A semiconductor device, according to claim 10, further including self-aligned silicide contacts over the other portion of at least one of the two regions.

4. A semiconductor device, according to claim 10, wherein each of the two regions include a relatively heavy doped area and a relatively lightly doped area, the dielectric extending over at least a portion of each relatively lightly doped area.

5. A semiconductor device, according to claim 10, wherein each of the two regions includes a relatively heavy doped area and a relatively lightly doped area, the dielectric extending over at least a portion of each relatively lightly doped area, and further including self-aligned silicide contacts over the relatively heavy doped area of at least one of the two regions.

6. A semiconductor device, according to claim 14, wherein the dopable region is doped to selectively link the two active regions.

7. A semiconductor device, according to claim 14, further including an area in the at least a portion of the dopable region adapted to prevent the two regions from being conductively linked.

8. A semiconductor device, according to claim 10, further including further including an area in the at least a portion of the dopable region adapted to prevent the two regions from being from being conductively linked.

9. A semiconductor device, according to claim 10, wherein each of the two regions does not include a relatively lightly doped area.

10. A semiconductor device, according to claim 1, wherein the dielectric is an oxide spacer.

11. A semiconductor device, according to claim 19, wherein the dopable region is configured and arranged to include at least one square of non-silicided LDD diffusion.

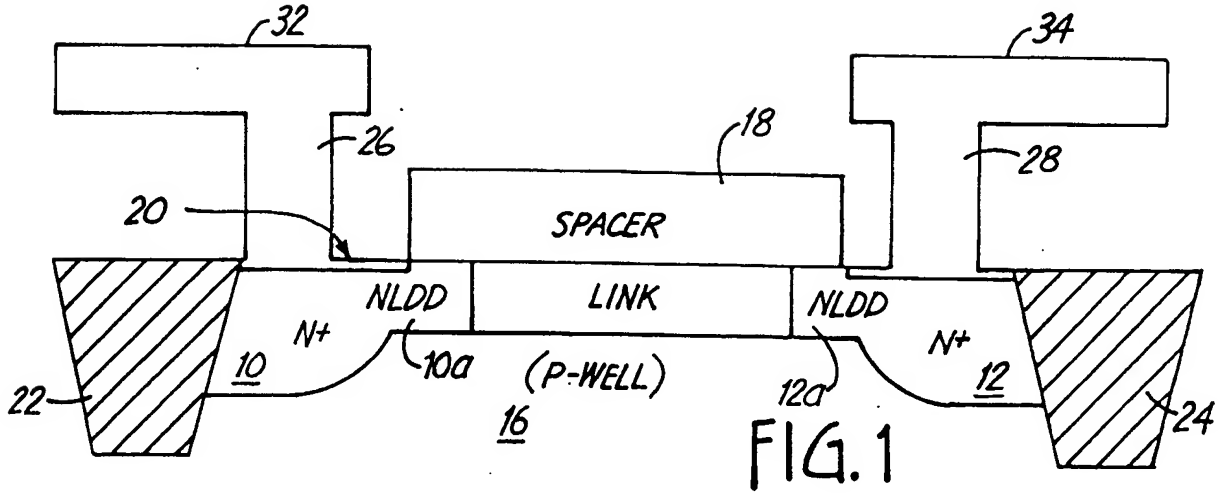

FIG. 1

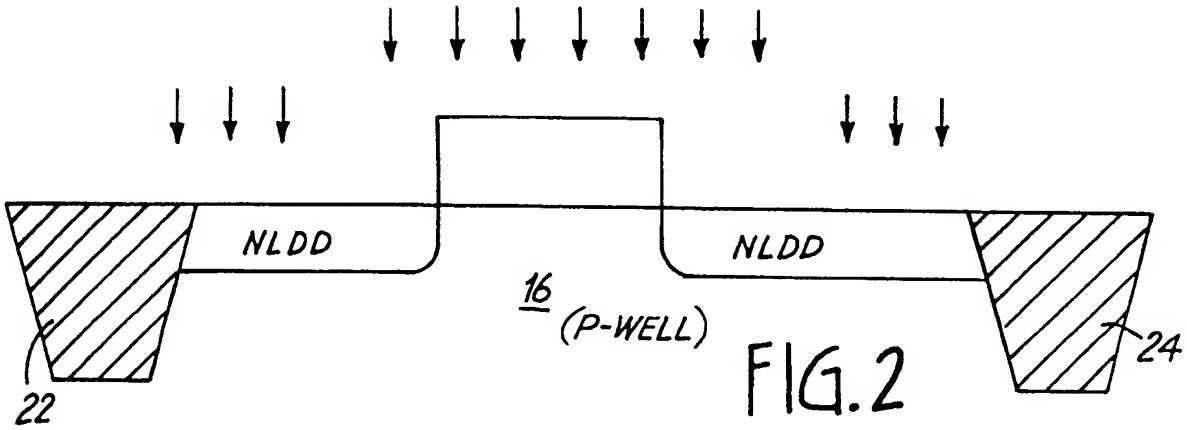

FIG. 2

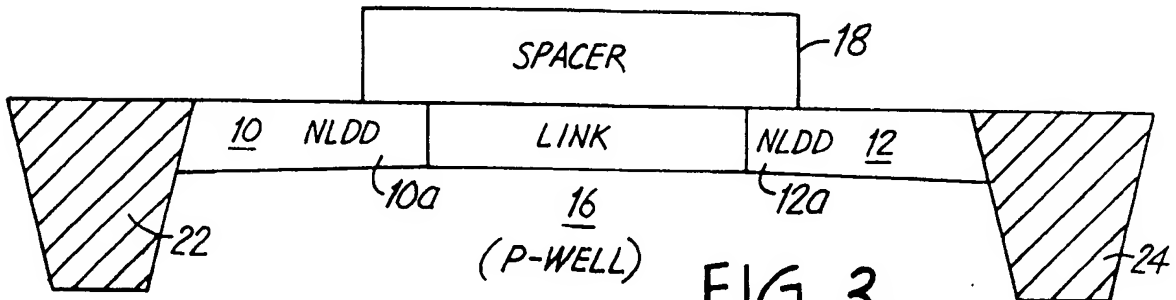

FIG. 3

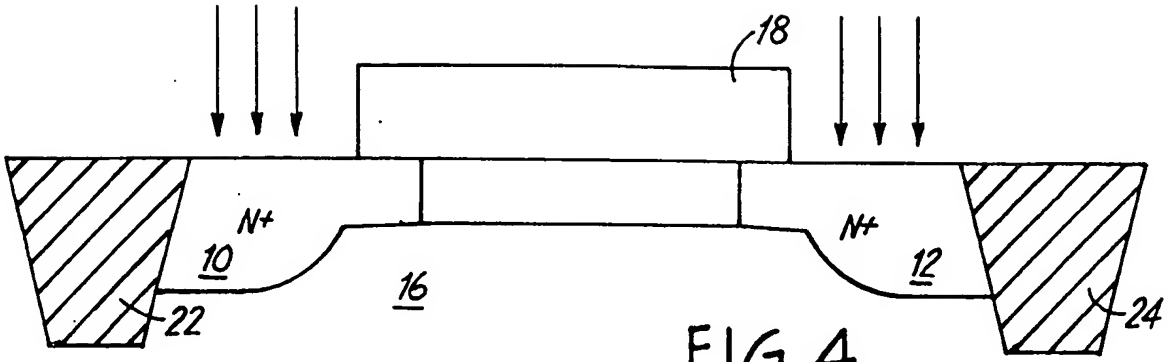

FIG. 4

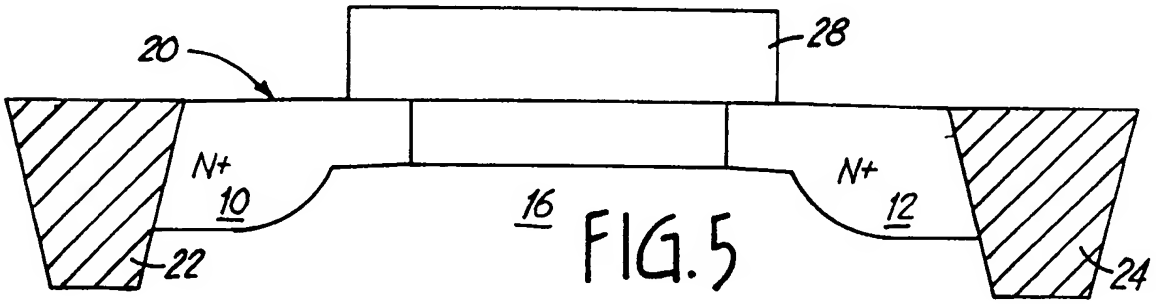

FIG. 5

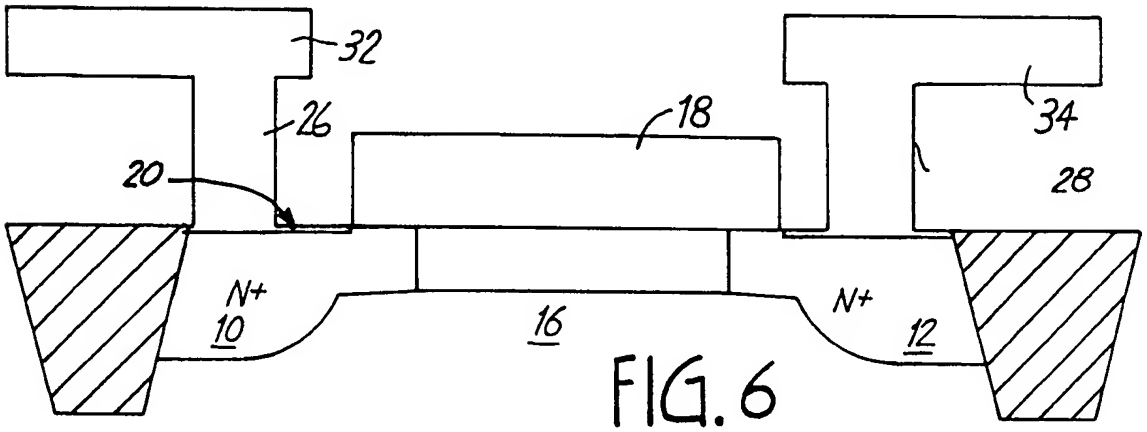

FIG. 6

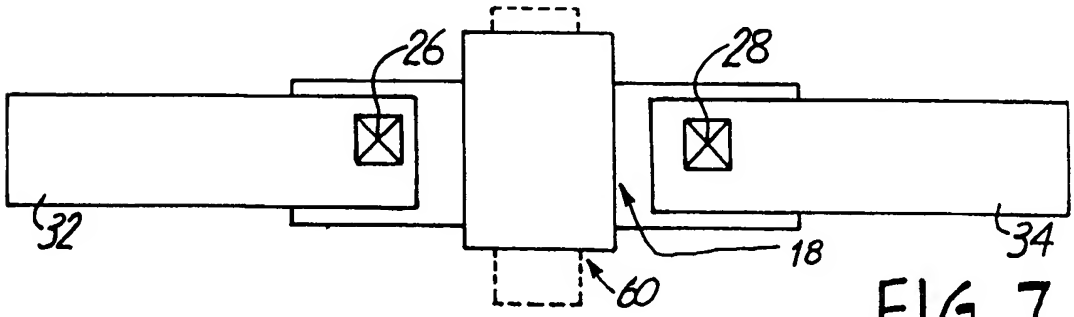

FIG. 7

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/02

According to International Patent Classification (IPC) or to both national classification and IPC

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 804 470 A (WOLLESEN DONALD L) 8 September 1998 (1998-09-08) figure 3	1,3-5, 7-11 2,6
X	WO 93 09567 A (VLSI TECHNOLOGY INC) 13 May 1993 (1993-05-13) figure 1	1,3-5, 7-11
X	US 5 834 356 A (PRAMANIK DIPANKAR ET AL) 10 November 1998 (1998-11-10) figure 7	1,3-5, 7-11
X	US 5 661 085 A (TEONG SU PING) 26 August 1997 (1997-08-26) figures 1B,5B	1,3-5, 7-11

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[X] Further documents are listed in the continuation of box C.

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Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 010 032 A (CHAPMAN RICHARD A ET AL) 23 April 1991 (1991-04-23) figure 4A	1,3-5, 7-11
Y	US 5 821 150 A (AHMAD AFTAB ET AL) 13 October 1998 (1998-10-13) column 4, line 19 - line 49; figures 7,8	2,6
A	WO 96 25765 A (PEREGRINE SEMICONDUCTOR CORP) 22 August 1996 (1996-08-22) page 26, line 9 - line 30; figures 4A,4B	1-11
A	PATENT ABSTRACTS OF JAPAN vol. 009, no. 069 (E-305), 29 March 1985 (1985-03-29) & JP 59 207652 A (HITACHI SEISAKUSHO KK), 24 November 1984 (1984-11-24) the whole document	2,6
A	US 5 465 005 A (STROTH LEO ET AL) 7 November 1995 (1995-11-07) figure 1	2,6

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. ..onal Application No
PCT/US 00/06346

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5804470 A	08-09-1998	EP 0958599 A	24-11-1999
		WO 9818158 A	30-04-1998
WO 9309567 A	13-05-1993	US 5411906 A	02-05-1995
US 5834356 A	10-11-1998	NONE	
US 5661085 A	26-08-1997	SG 66368 A	20-07-1999
		US 6025634 A	15-02-2000
US 5010032 A	23-04-1991	US 4821085 A	11-04-1989
		CN 1012310 B	03-04-1991
		CN 1043587 A,B	04-07-1990
		US 5065220 A	12-11-1991
		US 4890141 A	26-12-1989
		US 4971924 A	20-11-1990
		US 4931411 A	05-06-1990
		US 4975756 A	04-12-1990
		US 5302539 A	12-04-1994
		US 4804636 A	14-02-1989
		US 4657628 A	14-04-1987
		US 4676866 A	30-06-1987
		US 4894693 A	16-01-1990
		US 4811076 A	07-03-1989
		US 4811078 A	07-03-1989
		US 4814854 A	21-03-1989
US 5821150 A	13-10-1998	US 5940712 A	17-08-1999
		US 5668037 A	16-09-1997
		US 5780920 A	14-07-1998
WO 9625765 A	22-08-1996	JP 11500268 T	06-01-1999
		US 5864162 A	26-01-1999
		US 5930638 A	27-07-1999
JP 59207652 A	24-11-1984	NONE	
US 5465005 A	07-11-1995	US 5236857 A	17-08-1993